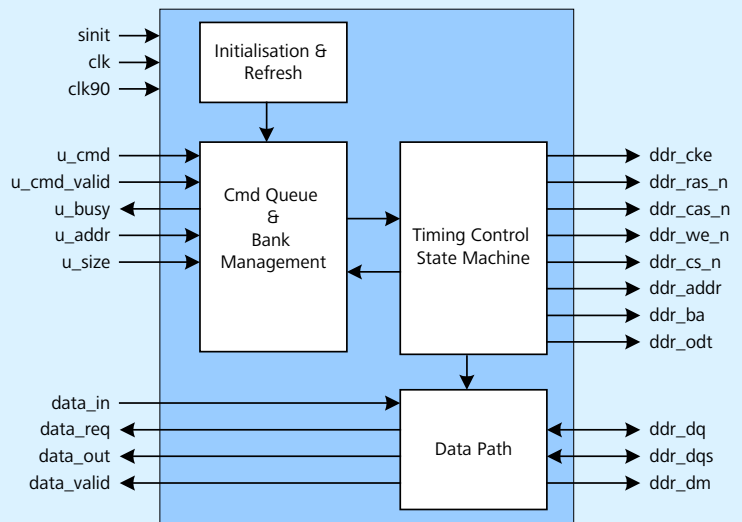


# DDR2 SDRAM Controller XS

For Xilinx® Programmable Logic Devices

## Features

- High performance memory access
- Available for Xilinx Virtex™-5, Virtex™-4, Spartan™-3 and Virtex™-II Pro FPGAs
- Full management of all 4 or 8 internal memory banks
- CAS latency, additive latency, burst length and all timing parameters configurable
- Optimised transaction processing with early activate, hidden precharge and posted read and writes
- Robust user application interface with split command and data buses
- Multi-ported user interface is an option
- Command queue architecture for high data throughput
- Adjustable controller pipeline delay to trade-off clock speed and access latency
- Read data capture optimized for Xilinx devices
- Uses Xilinx ChipSync™ technology in Virtex-5 and Virtex-4 devices for reliable read data capture
- Support all JEDEC standard DDR2 DIMMs and DDR2 SDRAM devices up to 4 Gbit
- Fully synchronous design without asynchronous resets



## Overview

The DDR2 SDRAM memory controller is a configurable high performance memory controller for systems requiring access to external DDR2 SDRAM memory devices with lowest latency and highest throughput. The controller consists of a high performance timing and control state machine that observes all timing requirements and issues the commands to the memory devices. The bank management module keeps track of the status of all the four internal banks to minimize activate and precharge times and achieve lowest latency. The command queue stores read or write requests until execution to optimize overall data throughput. There is no need to issue precharge, activate or refresh commands to the controller. All this functionality is handled internally by the controller.

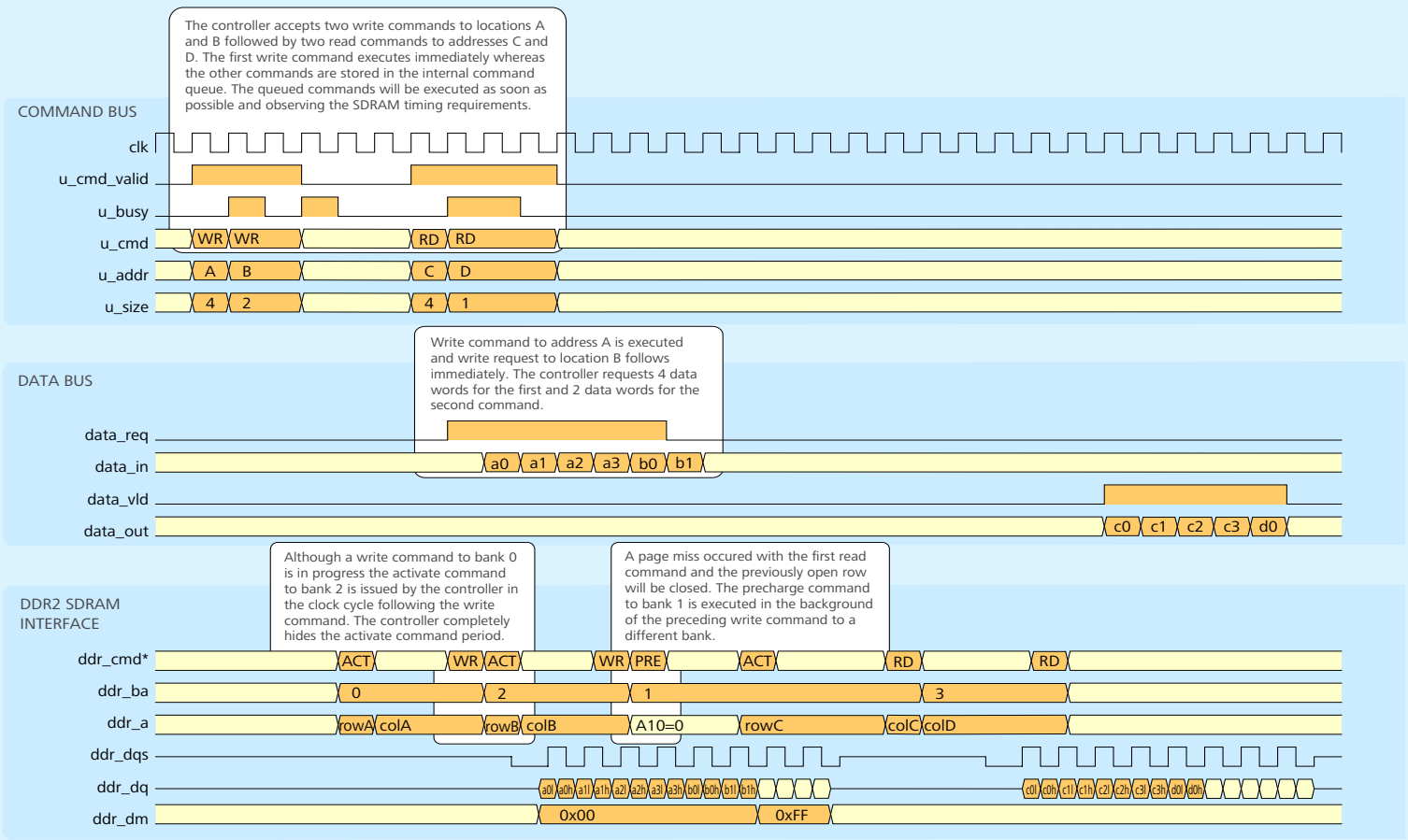
## User Interface

The user interface is split into separate command and data buses. This split allows for maximum flexibility while ensuring the highest performance during data transactions. Read and Write commands that are sent to the controller are registered in a small command

queue where they reside until the controller asserts a „busy“ signal. The busy signal will be deasserted once a command has been completed and there is space in the queue to accept another command. The amount of wait cycles that are introduced by the „busy“ signal are based on a dynamic flow control and are held as short as possible to prevent stall of command flow due to empty or full command queue. This results in increased overall throughput.

Write data associated with a write command is sent in contiguous cycles to the controller over a separate data bus. The write data does not have to be sent at the same time as the write command. The controller will start the write process once the associated write command is at the head of the queue. There is a „write data request“ signal output from the controller indicating at which time the controller requires the write data. The write data is then forwarded to the memory data bus with minimum latency.

When a read command is issued over the controller command bus, the associated read data is sent to the user logic over the separate data bus. A „read data valid“ signal from the controller indicates when the read data is available on the data bus. The data valid signal will be asserted for a number of contiguous clock cycles, consistent with the programmed burst length.



## Configurable Features

Many features of the DDR2 SDRAM Controller can be configured during synthesis time. The features that can be configured include:

- Data path size
- Number of chip selects
- Burst length of 4 or 8
- Memory timing parameters
- Row and column address sizes
- Controller pipeline delay

## Read Data Capture

In Virtex-5 and Virtex-4, two read data capture schemes are available which both use the incoming DQS signal to capture read data. Using the builtin ISERDES primitives provides highest data rates up to DDR667 at a slightly higher read latency. At lower data rates up to DDR466, the use of DDR registers provide the lowest read data capture latency.

## Address Mapping

The address bus from the user logic contiguously maps into the row, bank, column and chip select addresses of the memory devices. The following table shows the address mapping used in the controller.

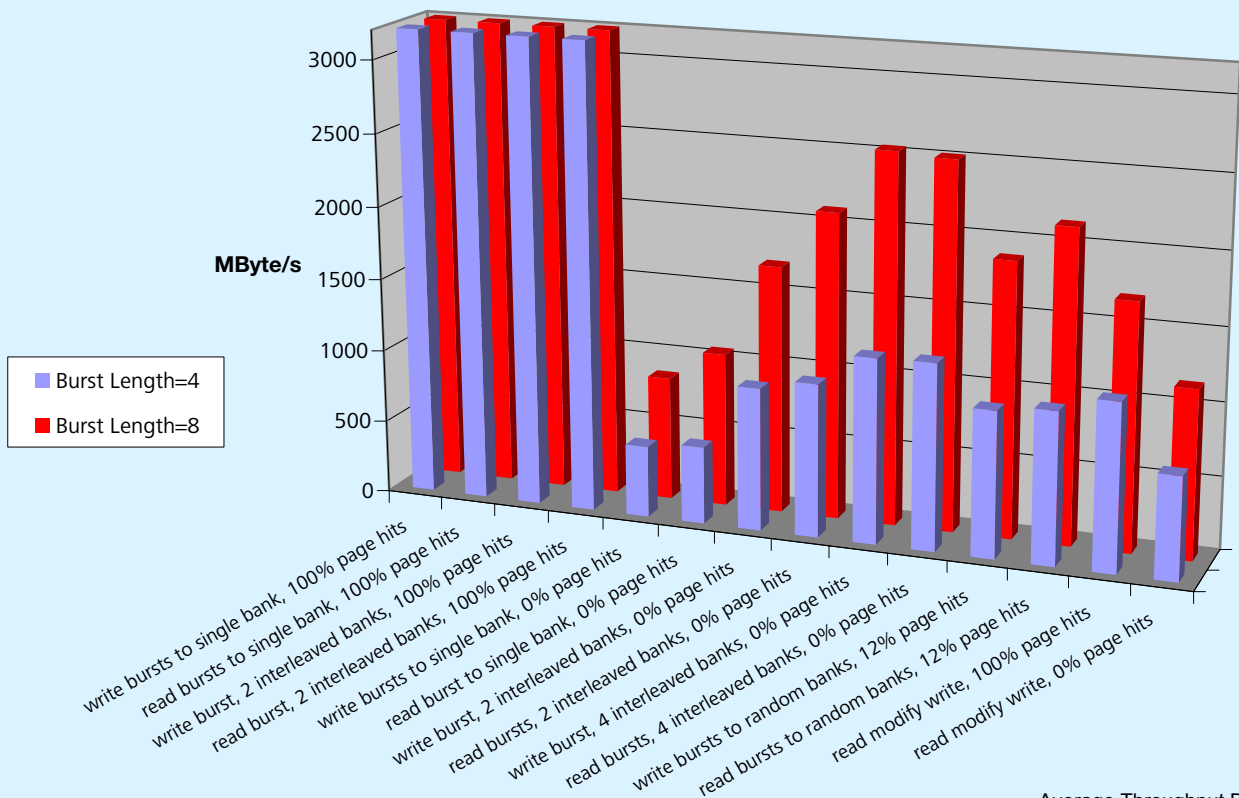
Address Mapping			
Logical User Address			
chip select	row	bank	column

## Speed and Size Summary

<b>Xilinx Virtex™-5</b>	
Slice FlipFlops / LUTs	690 / 600
DCM	1
BUFIO	8
internal clock speed <sup>(2)</sup>	280 MHz (-2 speedgrade)
external data rate <sup>(3)</sup>	DDR250 to DDR667
<b>Xilinx Virtex™-4</b>	
Slice FlipFlops / LUTs	690 / 770
Slices	570
DCM	1
BUFIO	8
internal clock speed <sup>(2)</sup>	250 MHz (-11 speedgrade)
external data rate <sup>(3)</sup>	DDR250 to DDR667
<b>Xilinx Spartan™-3</b>	
Slice FlipFlops / LUTs	900 / 800
Slices	680
DCM	2
internal clock speed <sup>(2)</sup>	145 MHz (-5 speedgrade)
external data rate <sup>(3)</sup>	DDR250 to DDR266
<b>Xilinx Virtex™-II Pro</b>	
Slice FlipFlops / LUTs	900 / 750
Slices	640
DCM	2
Clock Speed <sup>(2)</sup>	200 MHz (-6 speedgrade)
external data rate <sup>(3)</sup>	DDR250 to DDR333

Notes:

1. Configuration: 64 bit data bus, eight 128Mbx8 DDR2 SDRAMs, 8 managed banks and default controller pipeline latency.
2. This is the maximum internal clock frequency reported from static timing analysis and implementing the supplied reference design with Xilinx ISE 8.2.03i tools.
3. Maximum external data rate is affected by the design and layout of the printed circuit board and termination of high-speed signals.



Average Throughput Benchmark  
 Timing: 3-3-3@200 MHz  
 additive CAS latency = 2

## License Options

- Netlist project license: Core can be used on one project at customer site.
- Source code project license: Core can be used on one project at customer site.
- Source code site license: Core can be used on an unlimited number of designs at a customer site.



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## Deliverables

The netlist version of the core comes with:

- EDIF or NGC netlist
- pre-compiled simulation library for use with ModelSim simulator
- example design
- implementation scripts and constraints
- documentation
- 1 year of maintenance and support

The deliverables for a full source code license are:

- Verilog or VHDL source files
- comprehensive testbench
- example design
- implementation scripts and constraints
- documentation
- 1 year of maintenance and support

## Free Evaluation

For evaluation purposes a pre-compiled library for use with ModelSim simulator is available upon request.

## For More Information

We will be pleased to discuss how we can assist you with your individual requirements. Please contact Array Electronics to get more information or visit our website at: [www.array-electronics.com/cores](http://www.array-electronics.com/cores)



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