

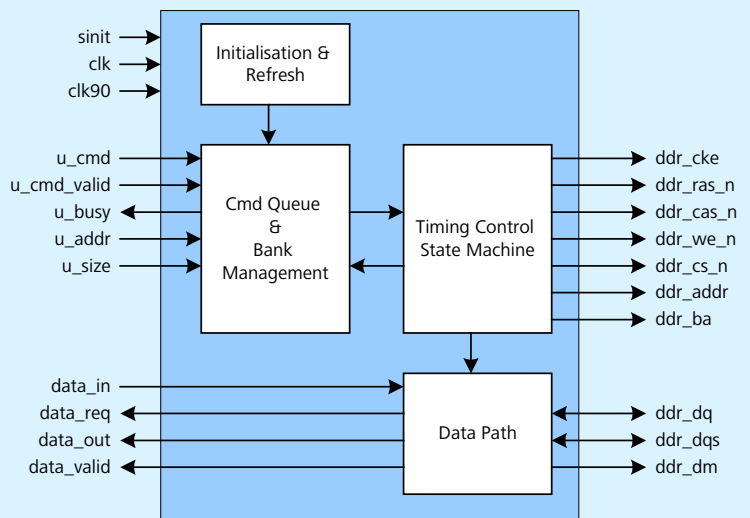
DDR SDRAM Controller XS

For Altera® Programmable Logic Devices



Features

- High performance memory access
- Available for Altera Stratix™ III, Stratix II, and Cyclone™ II FPGAs
- Full management of all 4 internal memory banks
- Optimised Transaction Processing with Early Activate and Hidden Precharge
- Command queue architecture
- CAS latency, burst length and all timing parameters configurable
- Generic user application interface with split command and data busses
- Dynamic burst sizing capability
- Optional multi-ported user interface
- ⊖ Read data capture optimized for Altera devices
- Multiple memory devices or DIMM support
- Support for DDR SDRAM devices from 64 Mbit to 1 Gbit
- Configurable controller latency to optimize latency/speed trade-off
- Fully synchronous design without asynchronous resets



Overview

The DDR SDRAM memory controller is a configurable high performance memory controller for systems requiring access to external DDR SDRAM memory devices with lowest latency and highest throughput. The controller consists of a high performance timing and control state machine that observes all timing requirements and issues the commands to the memory devices. The bank management module keeps track of the status of all the four internal banks to minimize activate and precharge times and achieve lowest latency. The command queue stores read or write requests until execution to optimize overall data throughput. There is no need to issue precharge, activate or refresh commands to the controller. All this functionality is handled internally by the controller.

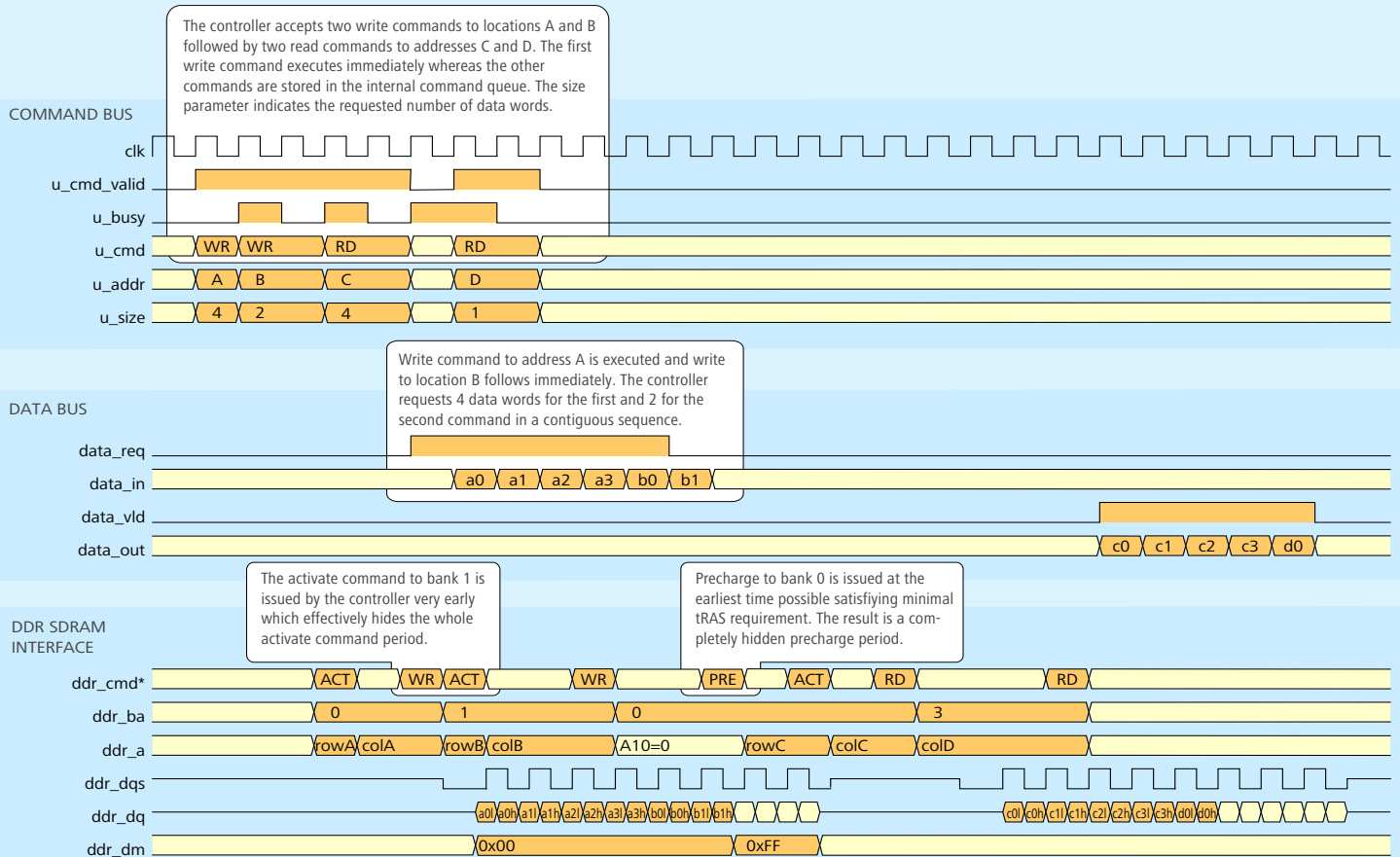
User Interface

The user interface is split into separate command and data busses. This split allows for maximum flexibility while ensuring the highest performance during data transactions. Read and Write commands that are sent to the controller are registered in a small command

queue where they reside until the controller asserts a „busy“ signal. The busy signal will be deasserted once a command has been completed and there is space in the queue to accept another command. The amount of wait cycles that are introduced by the „busy“ signal are based on a dynamic flow control and are held as short as possible to prevent stall of command flow due to empty of full command queue. This results in increased overall throughput.

Write data associated with a write command is sent in contiguous cycles to the controller over a separate data bus. The write data does not have to be sent at the same time as the write command. The controller will start the write process once the associated write command is at the head of the queue. There is a „write data request“ signal output from the controller indicating at which time the controller requires the write data. The write data is then forwarded to the memory data bus with minimum latency.

When a read command is issued over the controller command bus, the associated read data is sent to the user logic over the separate data bus. A „read data valid“ signal from the controller indicates when the read data is available on the data bus. The data valid signal will be asserted for a number of contiguous clock cycles, consistent with the programmed burst length.



Configurable Features

Many features of the DDR SDRAM Controller can be configured during synthesis time or during the operation of the controller. The features that can be configured include:

- Data path size
- Number of chip selects
- CAS Latency of 2.0, 2.5 or 3.0
- Burst length of 2, 4 or 8
- Refresh interval
- Memory timing parameters
- Row and Column Address Sizes
- Memory controller pipeline latency

Address Mapping

The address bus from the user logic contiguously maps into the row, bank, column and chip select addresses of the memory devices. The following table shows the address mapping used in the controller. This mapping achieves full bandwidth utilization for accesses with linear addressing scheme and for random accesses within a memory area that spans four contiguous rows.

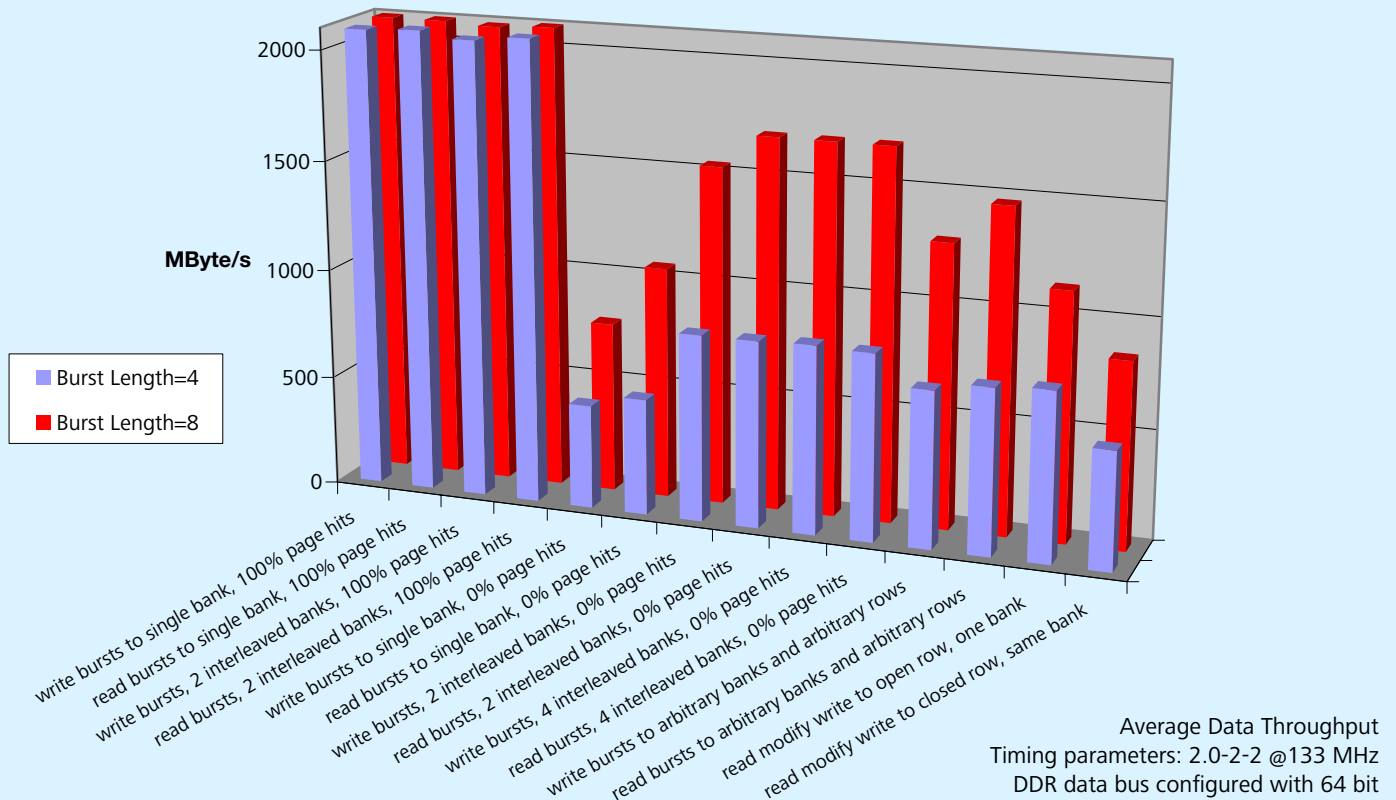
Address Mapping			
Logical User Address			
chip select	row	bank	column

Speed and Size Summary

Altera Stratix™ III	
Registers	650
Equivalent LEs	950
MLABs	2
PLLs	1
internal clock speed ⁽²⁾	250 MHz (-4 speedgrade)
external clock speed ⁽³⁾	DDR166 to DDR400
Altera Stratix™ II	
Registers	850
Equivalent Les	900
M512 RAM Blocks	2
PLLs	1
internal clock speed ⁽²⁾	230 MHz (-5 speedgrade)
external clock speed ⁽³⁾	DDR166 to DDR400
Altera Cyclone™ II	
Registers	850
Logic Elements	950
M4K RAM Blocks	1
PLLs	1
internal clock speed ⁽²⁾	166 MHz (-7 speedgrade)
external clock speed ⁽³⁾	DDR166 to DDR333

Notes:

1. Core configuration with 64 bit DDR SDRAM data bus.
2. This is the maximum clock frequency reported from static timing analysis and using Quartus II 5.0 implementation tools.
3. Maximum external data rate is affected by the design and layout of the printed circuit board and termination of high-speed signals.
4. Core netlist synthesized with Altera Quartus



License Options

- Netlist project license: Core can be used on one project at customer site.
- Source code project license: Core can be used on one project at customer site.
- Source code site license: Core can be used on an unlimited number of designs at a customer site.

Deliverables

The netlist version of the core comes with:

- EDIF netlist
- pre-compiled simulation library for use with ModelSim simulator
- example design and testbench
- implementation scripts and constraints
- documentation
- 1 year of maintenance and support

The deliverables for a source code license are:

- VHDL or Verilog source files
- comprehensive testbench
- example design
- implementation scripts and constraints
- documentation
- 1 year of maintenance and support

Free Evaluation

For evaluation purposes a pre-compiled library for use with ModelSim simulator is available upon request.

For More Information

We will be pleased to discuss how we can assist you with your individual requirements. Please contact Array Electronics or visit our website for more information:
www.array-electronics.com/cores



Hachinger Weg 5, 85649 Brunnthal, Germany, Tel. +49 (0)8102 779784, Fax +49 (0)8102 779785

Copyright © 2003-2006 Array Electronics. All rights reserved. All product names or company names mentioned herein and all logos are trademarks of their respective owners.

The product described in this document is subject to continuous development and Array Electronics reserves its right to change the document without notice. All particulars of the product and its use contained herein are given by Array Electronics in good faith. However, this document is provided "as-is" without warranty of any kind, either expressed or implied.

Printed in Germany. November 2006