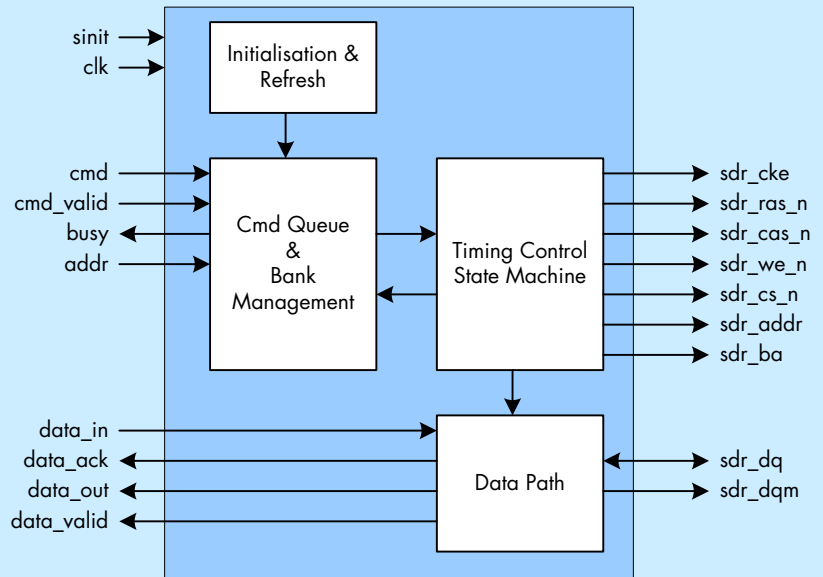


SDR SDRAM Controller

For Altera Programmable Logic Devices

Features

- High performance memory access for Single Data Rate (SDR) SDRAM and Mobile SDR SDRAM
- Available for Altera Stratix and Cyclone
- Full management of 2 or 4 internal memory banks
- Optimised Transaction Processing with Early Activate and Hidden Precharge
- Command queue with credit-based flow control for high data throughput
- CAS latency, burst length and all timing parameters configurable
- Generic user application interface with split command and data busses
- Fully synchronous design without asynchronous resets
- Support for data mask signals
- Supports Self Refresh
- Multiple memory devices or DIMM support
- Support for devices from 32 Mbit to 512 Mbit
- Optimised code achieves synthesis results with clock rates of more than 200 MHz



Overview

The SDR SDRAM memory controller is a configurable high performance memory controller for systems requiring access to external SDR SDRAM memory devices with lowest latency and highest throughput. The controller consists of a high performance timing and control state machine that observes all timing requirements and issues the commands to the memory devices. The bank management module keeps track of the status of all the four internal banks to minimize activate and precharge times and achieve lowest latency. The command queue stores read or write requests until execution to optimize overall data throughput. There is no need to issue precharge, activate or refresh commands to the controller. All this functionality is handled internally by the controller.

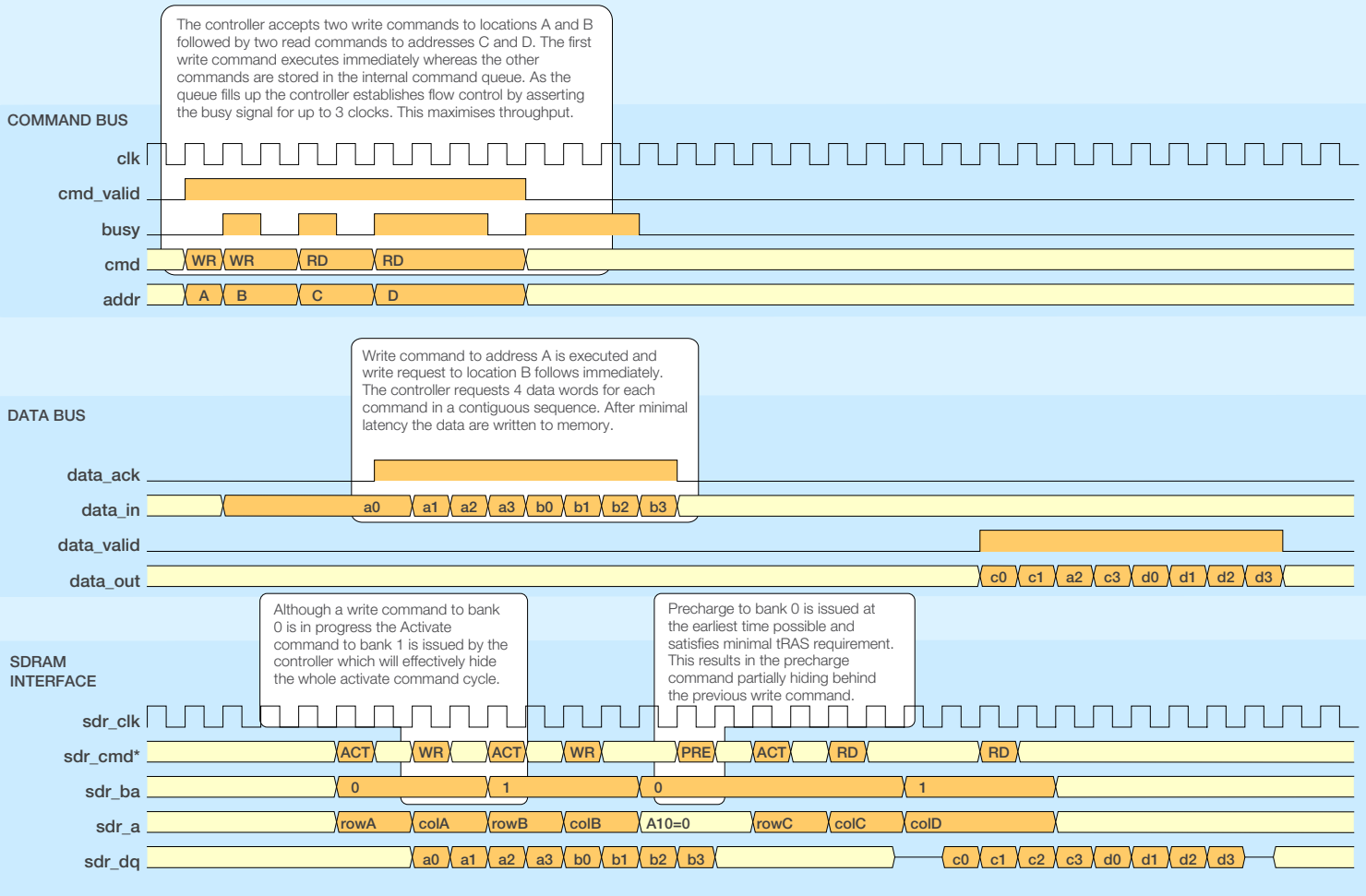
User Interface

The user interface is split into separate command and data busses. This split allows for maximum flexibility while ensuring the highest performance during data transactions. Read and Write commands that are sent to the controller are registered in a small command queue where they reside until the

controller asserts a „busy“ signal. The busy signal will be deasserted once a command has been completed and there is space in the queue to accept another command. The amount of wait cycles that are introduced by the „busy“ signal are based on a dynamic flow control and are held as short as possible to prevent stall of command flow due to empty or full command queue. This results in increased overall throughput.

Write data associated with a write command is sent in contiguous cycles to the controller over a separate data bus. The write data does not have to be sent at the same time as the write command. The controller will start the write process once the associated write command is at the head of the queue. There is a „write data request“ signal output from the controller indicating at which time the controller requires the write data. The write data is then forwarded to the memory data bus with minimum latency.

When a read command is issued over the controller command bus, the associated read data is sent to the user logic over the separate data bus. A „read data valid“ signal from the controller indicates when the read data is available on the data bus. The data valid signal will be asserted for a number of contiguous clock cycles, consistent with the programmed burst length.



Configurable Features

Many features of the SDR SDRAM Controller can be configured during synthesis time or during the operation of the controller. The features that can be configured include:

- Data path size
- Number of chip selects
- CAS Latency
- Burst length of 1, 2, 4 or 8
- Refresh interval
- Support for Self Refresh
- Memory timing parameters
- Row and Column Address Sizes

Address Mapping

The address bus from the user logic contiguously maps into the row, bank, column and chip select addresses of the memory devices. The following table shows the address mapping used in the controller. This mapping achieves full bandwidth utilization for accesses with linear addressing scheme and for random accesses within a memory area that spans four contiguous rows.

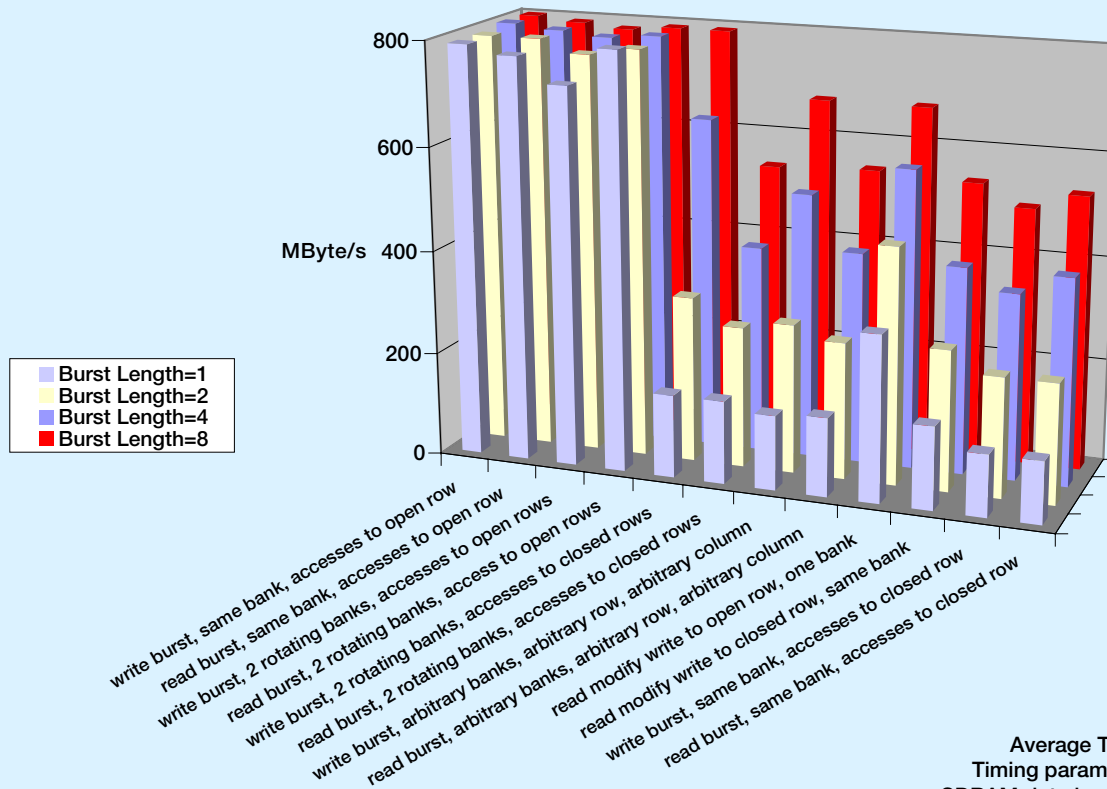
Address Mapping			
Logical User Address			
chip select	row	bank	column

Speed and Size Summary

Altera Stratix II⁽¹⁾	
Logic Cells	750
Registers	450
Memory bits	0
internal Clock Speed ⁽²⁾	220 MHz (-6 speedgrade)
	200 MHz
Synthesis Tools	Mentor Graphics, Quartus-II
Altera Stratix⁽¹⁾	
Logic Cells	750
Registers	450
Memory bits	0
internal Clock Speed ⁽²⁾	185 MHz (-6 speedgrade)
ext. SDRAM speed	166 MHz
Synthesis Tools	Mentor Graphics, Quartus-II
Altera Cyclone⁽¹⁾	
Logic Cells	750
Registers	450
Memory bits	0
internal Clock Speed ⁽²⁾	155 MHz (-7 speedgrade)
ext. SDRAM speed	133 MHz (-7 speedgrade)

Notes:

1. Configuration with 16 bit SDR SDRAM data bus, bank management with 4 banks and all parameters and address mapping hardcoded.
2. Maximum internal clock frequency achieved with an empty device.



Average Throughput Benchmark
Timing parameters: 2-2-2 @100 MHz
SDRAM data bus configured with 64 bit

License Options

- Single use EDIF netlist: Core can be used on one design at customer site
- Source code project license: Core can be used on one design at customer site
- Source code site license: Core can be used on an unlimited number of designs at a customer site.

Deliverables

The netlist version of the core comes with:

- EDIF netlist
- pre-compiled simulation library for use with ModelSim simulator
- example design
- implementation scripts and constraints
- documentation
- 1 year of maintenance and support
- During maintenance, new configurations of the EDIF netlist can be requested at no additional charge

The deliverables for a source code license are:

- VHDL or Verilog source files
- comprehensive testbench
- example design
- implementation scripts and constraints
- documentation
- 1 year of maintenance and support

Free Evaluation

For evaluation purposes a pre-compiled library for use with ModelSim simulator is available upon request.

For More Information

For more detailed information, please contact Array Electronics and we will be pleased to discuss how we can assist you with your individual requirements.

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