

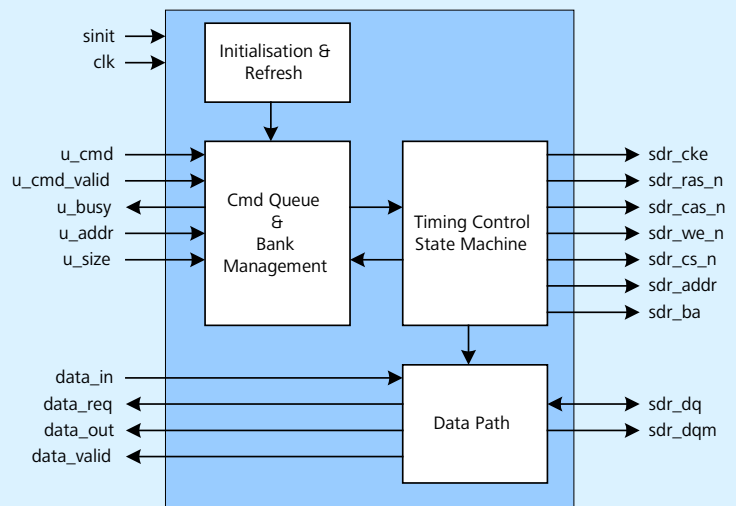
# SDR SDRAM Controller XS

For Xilinx® Programmable Logic Devices



## Features

- High performance memory access for Single Data Rate (SDR) SDRAM and Mobile SDR SDRAM
- Available for Virtex™-5, Virtex™-4, Virtex™-II Pro and Spartan™-3 FPGAs
- Full management of 2 or 4 internal memory banks
- Optimised transaction processing with early activate and hidden precharge
- Command queue with credit-based flow control for high data throughput
- CAS latency, burst length and all timing parameters configurable
- Generic user application interface with split command and data busses
- Supports Self Refresh
- Multiple memory devices or DIMM support
- Support for devices from 32 Mbit to 512 Mbit
- Fully synchronous design without asynchronous resets



## Overview

The SDR SDRAM memory controller is a configurable high performance memory controller for systems requiring access to external SDR SDRAM memory devices with lowest latency and highest throughput. The controller consists of a high performance timing and control state machine that observes all timing requirements and issues the commands to the memory devices. The bank management module keeps track of the status of all the four internal banks to minimize activate and precharge times and achieve lowest latency. The command queue stores read or write requests until execution to optimize overall data throughput. There is no need to issue precharge, activate or refresh commands to the controller. All this functionality is handled internally by the controller.

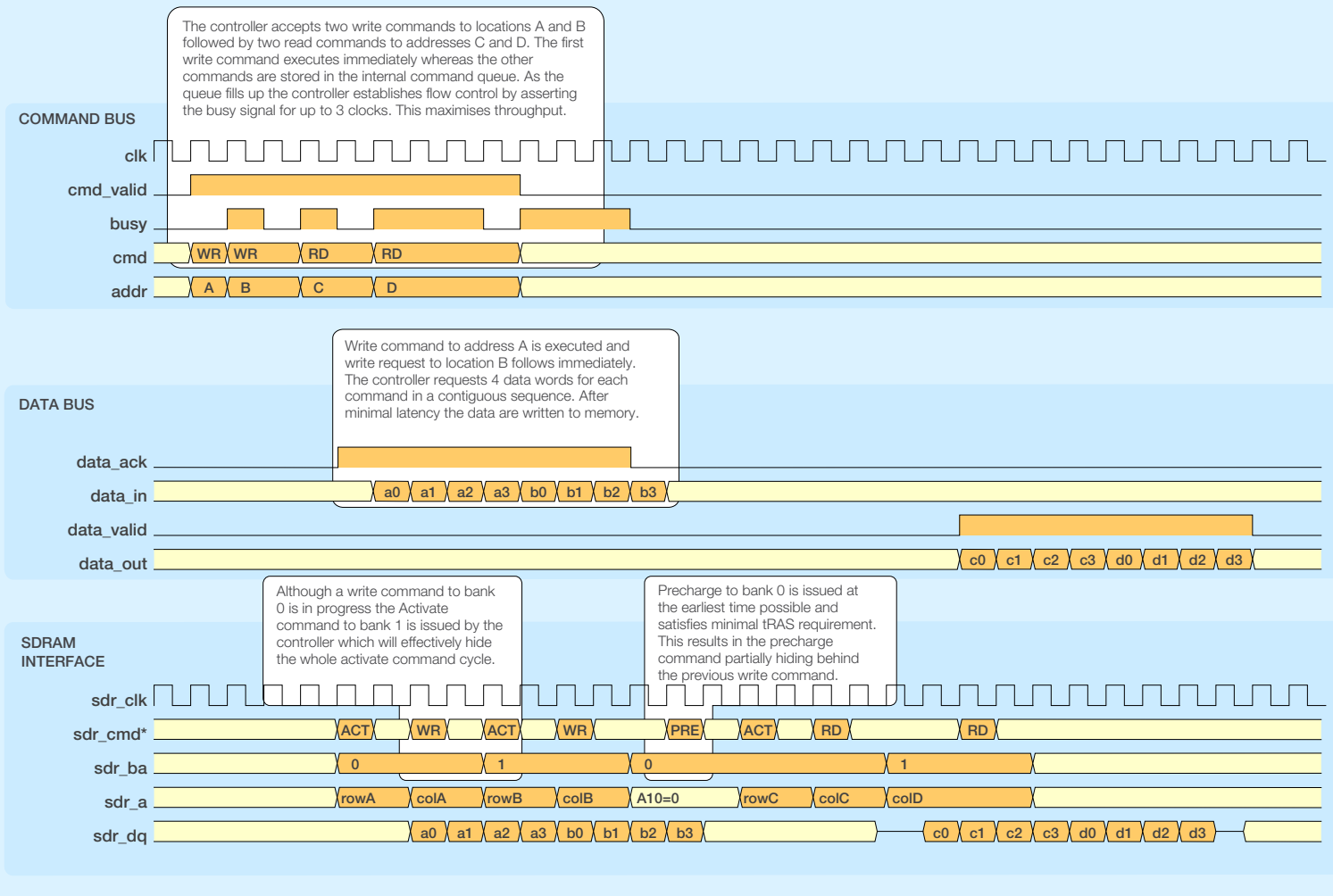
## User Interface

The user interface is split into separate command and data busses. This split allows for maximum flexibility while ensuring the highest performance during data transactions. Read and Write commands that are sent to the controller are registered in a small command queue where they reside until the controller asserts a

„busy“ signal. The busy signal will be deasserted once a command has been completed and there is space in the queue to accept another command. The amount of wait cycles that are introduced by the „busy“ signal are based on a dynamic flow control and are held as short as possible to prevent stall of command flow due to empty or full command queue. This results in increased overall throughput.

Write data associated with a write command is sent in contiguous cycles to the controller over a separate data bus. The write data does not have to be sent at the same time as the write command. The controller will start the write process once the associated write command is at the head of the queue. There is a „write data request“ signal output from the controller indicating at which time the controller requires the write data. The write data is then forwarded to the memory data bus with minimum latency.

When a read command is issued over the controller command bus, the associated read data is sent to the user logic over the separate data bus. A „read data valid“ signal from the controller indicates when the read data is available on the data bus. The data valid signal will be asserted for a number of contiguous clock cycles, consistent with the programmed burst length.



## Configurable Features

Many features of the SDR SDRAM Controller can be configured during synthesis time or during the operation of the controller. The features that can be configured include:

- Data path size
- Number of chip selects
- CAS Latency
- Burst length of 1, 2, 4 or 8
- Refresh interval
- Support for Self Refresh
- Memory timing parameters
- Row and Column Address Sizes

## Address Mapping

The address bus from the user logic contiguously maps into the row, bank, column and chip select addresses of the memory devices. The following table shows the address mapping used in the controller. This mapping achieves full bandwidth utilization for accesses with linear addressing scheme and for random accesses within a memory area that spans four contiguous rows.

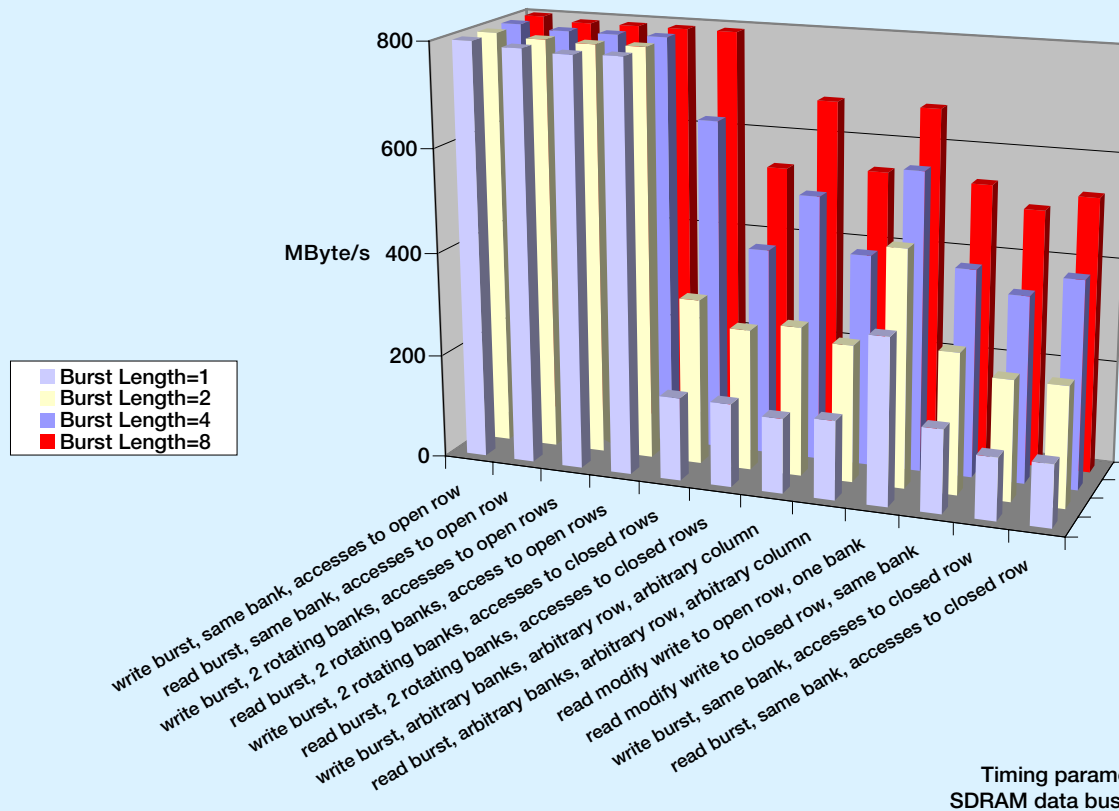
Address Mapping			
Logical User Address			
chip select	row	bank	column

## Speed and Size Summary

Device	Virtex™-5	Virtex™-4	Virtex™-II Pro	Spartan™-3	Virtex™-E	Spartan™-2E
Slice FlipFlops	295	295	295	310	295	295
LUTs	347	440	425	405	420	420
SRL16	25	25	23	25	25	25
Slices	426	265	255	250	245	245
IOB FlipFlops	116	116	116	116	116	116
IOBs	56	56	56	56	56	56
BUFGs	1	1	1	1	1	1
fMAX	210 (-1)	225 MHz (-11)	200 MHz (-6)	124 MHz (-4)	115 MHz (-7)	100 MHz (-6)

Notes:

1. Configuration with 32 bit SDRAM data bus.
2. fMAX is the maximum internal clock frequency achieved with an empty device and reported from static timing analysis. Speedgrade is given in parentheses after device family.
3. Synthesis and place-and-route results achieved using ISE 8.1.03i implementation tools.
4. Synthesis and place-and-route results for Virtex-5 device are preliminary values obtained using ISE 8.2.01i tools.



## License Options

- Single use EDIF netlist: Core can be used on one project at customer site
- Source code project license: Core can be used on one project at customer site
- Source code site license: Core can be used on an unlimited number of designs at a customer site.



Array Electronics is a member of the Common License Consortium and supports the SignOnce IP License. Refer to <http://www.xilinx.com/ipcenter/signonce.htm> for more information about the SignOnce IP License.

## Deliverables

The netlist version of the core comes with:

- EDIF or NGC netlist
- pre-compiled simulation library for use with ModelSim simulator
- example design and testbench
- implementation scripts and constraints
- documentation
- 1 year of maintenance and support

- During maintenance, new configurations of the EDIF netlist can be requested at no additional charge

The deliverables for a source code license are:

- VHDL or Verilog source files
- comprehensive testbench
- example design
- implementation scripts and constraints
- documentation
- 1 year of maintenance and support

## Free Evaluation

For evaluation purposes a pre-compiled library for use with ModelSim simulator is available upon request.

## For More Information

For more detailed information, please contact Array Electronics and we will be pleased to discuss how we can assist you with your individual requirements. Or visit us at: [www.array-electronics.com/cores](http://www.array-electronics.com/cores)



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